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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,596	12/31/2001	Howard S. David	42390.P13873	2205

8791 7590 09/17/2003

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2186	4

DATE MAILED: 09/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,596	DAVID, HOWARD S.	
	Examiner	Art Unit	
	Zhuo H Li	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

Page 6 lines 4-5, "the DRAM is placed on a motherboard rather that on a memory module" should be -- the DRAM is placed on a motherboard rather than on a memory module--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4 and 13-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Saulsbury et al. (US PAT. 6,128,702 hereinafter Saulsbury).

Regarding claim 1, Saulsbury discloses an apparatus (100, figure 1) comprising an array, i.e., primary data cache bank tag/flag storage, (148, figure 2) of tag address storage locations (col. 7 lines 42-61), and a command sequencer and serializer unit, i.e., primary data cache bank logic, (150, figure 2) coupled to the array of tag address storage locations (figure 2), the command sequencer and serialize unit to control a data cache i.e., primary data cache bank N (122, figure 2) associated with a memory module, i.e., memory block N (104, figure 2), the

command sequencer and serializer unit to cause a current line of data to be write from the command sequencer and serializer unit to the data cache (col. 11 lines 15-47).

Regarding claim 2, Saulsbury discloses the command sequencer and serializer unit to cause a previous line, i.e., victim data cache line, of data to be evicted out of the data cache to an eviction buffer, i.e., victim data cache, located on the memory module (col. 11 line 47 through col. 12 line 6 and col. 12 line 48 through col. 13 line 66).

Regarding claim 3, Saulsbury discloses the command sequencer and serializer to deliver a writeback command to the data cache associated with the memory module, the write back command to cause the previous line of data stored in the eviction buffer to be written out to a memory module memory device (col. 12 line 48 through col. 13 line 66 and col. 14 lines 37-64).

Regarding claim 4, Saulsbury discloses the writeback command including way information and bank address information (col. 12 line 48 through col. 13 line 66 and col. 14 lines 37-64).

Regarding claim 13, Saulsbury discloses a method comprising writing a current line of data from a memory controller, i.e., data cache bank logic (150, figure 2), to a data cache, i.e., primary data cache bank N (122, figure 2) location on a memory module, i.e., memory device (103, figure 1) and (col. 11 lines 15-47), evicting a previous line of data from the data cache to an eviction buffer, i.e., victim cache (106, figure 1) on the memory module (col. 11 line 47 through col. 12 line 6), and writing the previous line of data from the eviction buffer to a memory device is not busy (col. 12 line 48 through col. 13 line 66).

Regarding claim 14, Saulsbury discloses the method wherein writing the previous line of data from the eviction buffer to the memory device includes receiving a writeback command from a memory controller at the data cache (col. 12 line 48 through col. 13 line 66).

Regarding claim 15, Saulsbury discloses the method wherein receiving a writeback command includes receiving way information and bank address information (col. 12 line 48 through col. 13 line 66 and col. 14 lines 37-64).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saulsbury et al. (US PAT. 6,128,702 hereinafter Saulsbury) in view of Westberg (US PAT. 5,361,391).

Regarding claim 5, Saulsbury discloses an apparatus (104, figure 2) comprising at least one memory device, i.e., memory bank N (118, figure 2) and instruction cache bank N (120, figure 2) and primary data cache bank N (122, figure 2), and a data cache, i.e., primary data cache (122) coupled to the memory device via the cache line bus (4096), the data cache controlled by a plurality commands delivered by a memory controller, i.e., primary data cache bank logic (150, figure 2) component over a memory bus, i.e., cache line bus (4096) and control bus as indicated on figure 2, and the memory controller writing a current line of data to the data

cache (col. 11 lines 15-47). Saulsbury differs from the claimed invention in not specifically teaches the memory controller component including an array of tag address storage locations. However, Westberg teaches in the computer system (10, figure 1) comprising a memory controller (14, figure 1) which including two tag array (30a and 30b, figure 2), and each tag is corresponding to the data cache line (col. 4 lines 34-44). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory controller in the apparatus of Saulsbury in having an array of tag address storage locations which corresponding to the data cache line at primary data cache bank, as per teaching of Westberg, because it reduces CPU idle time and improves the computer system performance.

Regarding claim 6, Saulsbury discloses the memory controller further instructing the data cache to evict a previous line of data from the data cache into an eviction buffer (col. 11 line 47 through col. 12 line 6 and col. 12 line 48 through col. 13 line 66).

Regarding claim 7, Saulsbury discloses the memory controller to deliver a writeback command to the data cache, the write back command to cause the previous line of data to be written out of the eviction buffer to the memory device (col. 12 line 48 through col. 13 line 66 and col. 14 lines 37-64).

Regarding claim 8, Saulsbury discloses the writeback command including way information and bank address information (col. 12 line 48 through col. 13 line 66 and col. 14 lines 37-64).

6. Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Westberg (US PAT. 5,361,391) in view of Saulsbury et al. (US PAT. 6,128,702 hereinafter Saulsbury).

Regarding claim 9, Westberg discloses a system (10, figure 1) comprising a processor (12, figure 1), a memory controller (14, figure 1) coupled to the processor via the address bus 22 and data bus 24, the memory controller including an array of tag address storage locations, i.e., tag array A (30a) and tag array B (30b) in figure 2, and a command sequencer and serializer unit, i.e., control logic (28, figure 2) coupled the array of tag address storage locations (figure 2 and col. 4 lines 34-44), and memory module (16, figure 2) coupled to the memory controller (figure 2 and col. 3 line s 33-48). Westberg differs from the claimed invention in not specifically teaches the memory module including at least one memory device, and a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by the memory controller, the memory controller writing a current line of data to the data cache. However, Saulsbury teaches the computer system (100, figure 1) comprising a memory system (103) which including a plurality of memory block (15), i.e., memory modules, and each memory module further comprising a memory device, i.e., memory bank N (118, figure 2) and a data cache, i.e., primary data cache bank N (122, figure 2), the data cache is coupled to the memory device via the cache line bus (4096), and the data cache controlled by a plurality of commands delivered by the memory controller, i.e., primary data cache bank logic (150, figure 2), which the memory controller writing a current line of data to the data cache (col. 11 lines 15-47). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the memory module in the computer system of Westberg in having at least one memory device, and a data cache coupled to the memory device, the data cache controlled by a plurality of commands delivered by the memory controller, the memory controller writing a

current line of data to the data cache, as per teaching of Saulsbury, because it reduces the miss rate and increase the access speed of in the memory operation.

Regarding claim 10, the limitations of the claim are rejected as the same reasons set forth in claim 6.

Regarding claim 11, the limitations of the claim are rejected as the same reasons set forth in claim 7.

Regarding claim 12, the limitations of the claim are rejected as the same reasons set forth in claim 8.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

McAllister et al. (US PAT. 6,463,506) discloses arrangement of data within cache lines so that tags first data received (abstract).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H Li whose telephone number is 703-305-3846. The examiner can normally be reached on Tue-Fri 9:00 a.m. to 6:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 703-305-3821. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Zhuo H. Li
September 5, 2003

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
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